1. Read request from L1 data.
   1. Hit
      1. Exclusive
         1. MESI - Stays E
            1. Pass data to L1 Data
      2. Modified   
         a. MESI - Stays M   
         b. Pass data to L1 Data   
         iii. Invalid   
         a. HIT   
         i. MESI - Shared   
         ii. Get data from shared bus   
         b. MISS (HIT')   
         i. MESI - Exclusive   
         ii. Get data from shared bus   
         iv. Shared   
         a. MESI - Shared   
         b. Pass data to L1 Data   
         c. Miss   
         i. Read data from shared bus   
         ii. Place in L2.   
         iii. Pass to L1 Data.
2. Write request from L1 data
   1. Hit
      1. Exclusive
         1. MESI – Modified
         2. Write to L2 cache
      2. Modified
         1. MESI - Modified
         2. Write to L2 cache
      3. Invalid
         1. MESI – Modified
         2. Read from shared bus with RFO
         3. Write to L2 cache
      4. Shared
         1. MESI – Modified
         2. Read from shared bus with RFO or Invalidate
         3. Write to L2 cache
   2. Miss
      1. Read from shared bus with RFO
3. Read request from L1 instruction
   1. Same as Read request from L1 data
   2. Snooped invalid command (Reading from shared bus)
      1. Wait for data to be loaded from processor owning data to the bus/ram
4. Snooped read request (someone is trying to read)
   1. Hit
      1. M
      2. E
      3. S
      4. I
   2. Miss
      1. Put miss
5. Snooped write request   
   a. Hit   
   b. HitM   
   c. Miss
6. Snooped read with intent to modify   
   a. Hit   
   b. Miss
7. Clear and reset all   
   a.
8. Print contents and state of each valid line   
   a.